REMARKS

I. THE SHIFT AMPLIFIER 22 IS A COMBINING UNIT AND NOT A COMPARING UNIT, AND THUS "COMBINING" OR A SIMILAR TERM SHOULD REMAIN IN CLAIM 1

The shift amplifier 22 is a combining unit and not a comparing unit. The Summary of the Invention section (paragraph 0007 of the published application) states:

> "The present invention is achieved by continuously providing a shift voltage SV(t) to one input terminal of a two input terminal shift amplifier whose other input terminal is fed with a pulsed analog data voltage ADV(t) corresponding to incoming digital data pulses for issuing a *summed up* pulsed drive voltage DV(t)."

This means, of course, that the function of this element 22 is to *sum up* the two input voltages it sees at its terminals and output these as summed up voltage DV(t) for further processing down the line. The "shift amplifier" in the invention is actually, and is as drawn, an operational amplifier (well known in the electronics art) that adds/combines electronic signals appearing on its terminals.

Paragraph 19 of the published specification also states:

> "The shift amplifier 22 has an inverting input terminal 28 connected to the fan out buffer 21 for receiving analog data voltage ADV(t) corresponding to the negative digital data pulses emanating from the fan out buffer 21, and an input terminal 29 connected to the integrating unit 26 for receiving a variable shift voltage SV(t) whereupon the *shift amplifier 22 algebraically adds by superposition* the analog data voltage ADV(t) and the shift voltage SV(t) to output a *summed up* drive voltage DV(t)."

Further, it is clear from drawings 4 and 5 of the application that these 2 voltages, i.e., ADV(t) and SV(t) are *summed up* to receive a combined output.

The function of the shift amplifier is clearly not to compare, since the function of comparison typically issues out an ON/OFF or LARGER THAN/SMALLER THAN "answer", such as is done by comparator 33 in the circuit (see paragraph 20 of the published specification which states: "... The comparator 33 outputs either an ON or OFF digital control state to the integrating unit 26"). The shift amplifier does not issue an ON/OFF signal but rather a continuous signal (as apparent from the drawings) that is a combination of the signals appearing on its 2 input terminals.

As an alternative to leaving the term "combining" in Claim 1, Applicant would agree to an examiner's amendment that replaces "combining" with "algebraically superimposing". Support for such an amendment is found in paragraph 19 of the published specification as discussed above, and in original Claim 7.

II. CLAIM 2 CORRECTION

Claim 2 has been amended to specify that the first mentioned digital control state is an ON digital control state. Previously, Claim 2 merely stated that the first mentioned digital control state is a digital control state, and while it is technically true that the ON digital control state is a digital control state, it is more correct and clear to specify that the first mentioned digital control state is an ON digital control state. This correction also fits better with the claim language immediately following the correction, which states that the second mentioned digital control

state is an *opposite* OFF digital control state. Since ON is the opposite of OFF, correcting Claim 2 in this manner makes the claim clearer and more definite.

The Claim 2 amendment is fully supported in the specification, for example at paragraph 20 of the published application:

> "The comparator 33 outputs either an ON or OFF digital control state to the integrating unit 26 as follows: the comparator 33 outputs an ON digital control state when V.sub.REF>FV(t) (see FIG. 3B) and conversely an OFF digital control state when FV(t)>V.sub.REF (see FIGS. 3C and 3D). FIG. 3C and FIG. 3D show that the maximum voltage of the filtered voltage pulses dictates the duration that FV(t)>V.sub.REF and consequently the duration that the comparator 33 issues the OFF digital control state. The comparator 33 issues a longer OFF digital control state T2>T1 for the voltage pulse shown in FIG. 3D than that shown in FIG. 3C."

III. SPECIFICATION CORRECTION

Paragraph 21 of the published specification has been corrected to clarify that the discharge of the capacitive memory component 42 occurs *swiftly* (i.e. relative to the charging of the capacitive memory component), instead of *slowly* as in the original specification. This error in the original specification, and the appropriate correction which has been made herein, is apparent from the timing diagrams in Fig. 4 and 5.

CONCLUSION

For all the above reasons, Applicant requests that "combining", or the similar term "algebraically superimposing", remain in Claim 1, and that the corrections to Claim 2 and the specification be entered into the application.

Respectfully,

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